EXHIBIT V

Exhibit 14 – TI TMS320C32

'156 Patent

Claim Limitation (Claim 7)	Exemplary Disclosure
[**156a**] A device comprising:	TI TMS320C32 discloses a device. Specifically, the TI TMS320C32 is a chip for digital signal processing. *See, e.g.*:  **1.1.4 TMS320C32** The 'C32 is the newest member of the 'C3x generation. They are enhanced versions of the 'C3x family and the lowest cost floating-point processors on the market today. These enhancements include a variable-width memory interface, two-channel DMA coprocessor with configurable priorities, flexible boot loader, and a relocatable interrupt vector table. TMS320C3x User's Guide 1-4.

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Claim Limitation (Claim 7)	Exemplary Disclosure

Device Name	Freq (MHz)	Cycle Time (ns)	Memory (words) On-Chip RAM	On-Chip ROM	On-Chip Cache	Off-Chip Parallel	Peripherals Serial	Peripherals DMA Channels	Peripherals Timers	Package Type
'C32 (5 V)	40	50	512	Boot loader	64	16M × 32/16/8	1	2	2	144 PQFP
	50	40	512	Boot loader	64	16M × 32/16/8	1	2	2	144 PQFP
	60	33	512	Boot loader	64	16M × 32/16/8	1	2	2	144 PQFP

TMS320C3x User's Guide 1-6.

2.1 Overview

The 'C3x architecture responds to system demands that are based on sophisticated arithmetic algorithms that emphasize both hardware and software solutions. High performance is achieved through the precision and wide dynamic range of the floating-point units, large on-chip memory, a high degree of parallelism, and the DMA controller.

Figure 2–1 through Figure 2–3 show functional block diagrams of the 'C30, 'C31, and 'C32 architectures, respectively.

TMS320C3x User's Guide 2-2.

That the TI TMS320C32 is a chip is reflected in various other documents, including the TMS320C3x User's Guide, TMS320C3x General-Purpose Applications User's Guide, TMS320C32 Digital Signal Processor Data Sheet, and Interfacing Memory to the TMS320C32 DSP.

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Claim Limitation (Claim 7)	Exemplary Disclosure
[**156b**] at least one first low precision high dynamic range (LPHDR) execution unit adapted to execute a first operation on a first input signal representing a first numerical value to produce a first output signal representing a second numerical value,	TI TMS320C32 discloses at least one first low precision high dynamic range (LPHDR) execution unit adapted to execute a first operation on a first input signal representing a first numerical value to produce a first output signal representing a second numerical value. *See, e.g.*: **2.1 Overview** The 'C3x architecture responds to system demands that are based on sophisticated arithmetic algorithms that emphasize both hardware and software solutions. High performance is achieved through the precision and wide dynamic range of the floating-point units, large on-chip memory, a high degree of parallelism, and the DMA controller. Figure 2–1 through Figure 2–3 show functional block diagrams of the 'C30, 'C31, and 'C32 architectures, respectively. TMS320C3x User's Guide 2-2. In addition to integer formats, the TMS320C32 took input signals representing a first numerical value and provided output signals representing a second numerical value in floating-point formats:

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Claim Limitation (Claim 7)	Exemplary Disclosure

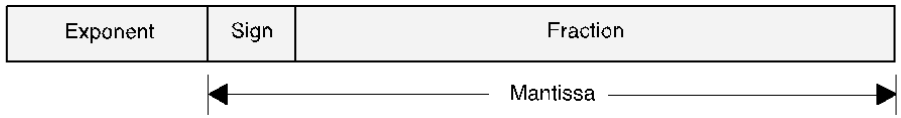
5.3 Floating-Point Formats

The 'C3x supports four floating-point formats:

- A short floating-point format for immediate floating-point operands, consisting of a 4-bit exponent, a sign bit, and an 11-bit fraction
- ('C32 only) A short floating-point format for use with 16-bit floating-point data types, consisting of a 2s-complement, 8-bit exponent field, a sign bit, and a 7-bit fraction
- A single-precision floating-point format by an 8-bit exponent field, a sign bit, and a 23-bit fraction
- An extended-precision floating-point format consisting of an 8-bit exponent field, a sign bit, and a 31-bit fraction.

All 'C3x floating-point formats consist of three fields: an *exponent* field *(e)*, a *single-bit sign* field *(s), and a fraction* field *(f)*. The sign field and fraction field may be considered as one unit and referred to as the *mantissa* field (*man*).

Figure 5–5. General Floating-Point Format



TMS320C3x User's Guide 5-4.

Notably, this included a format specific to the C32 chip "A short floating-point format for use with 16-bit floating-point data types, consisting of a 2s-complement, 8-bit exponent field, a sign bit, and a 7-bit fraction." TMS320C3x User's Guide 5-4.

Exhibit 14 – TI TMS320C32

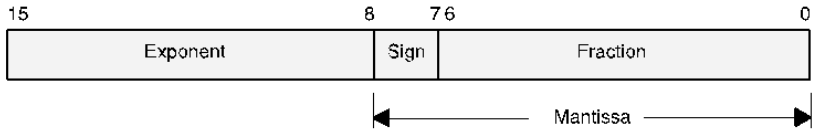
Claim Limitation (Claim 7)	Exemplary Disclosure

5.3.2 TMS320C32 Short Floating-Point Format for External 16-Bit Data

To facilitate the handling of 16-bit floating-point data types, the 'C32 uses a new short floating-point format for external 16-bit data types. Note that the following short floating-point format is used only in external 16-bit floating-point data access. This format is different than the 16-bit immediate short floating-point data format used in the 'C32's instruction set.

In the short floating-point format for external 16-bit data-type size, floating-point numbers are represented by a 2s-complement, 8-bit exponent field (*e*), a sign bit (*s*), and an 8-bit mantissa field (*man*) with an implied most significant nonsign bit.

Figure 5–7. TMS320C32 Short Floating-Point Format for External 16-Bit Data



Operations are performed with an implied binary point between bits 7 and 6. When the implied most significant nonsign bit is made explicit, it is located to the immediate left of the binary point. The floating-point 2s-complement number *x* in the short floating-point format is given by:

$x = 01.f \times 2^e$ if $s = 0$
$x = 10.f \times 2^e$ if $s = 1$
$x = 0$ if $e = -128$

You must use the following reserved values to represent 0 in the 'C32 short floating-point format for external 16-bit data:

$e = -128$
$s = 0$
$f = 0$

TMS320C3x User's Guide 5-6.

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<table>
<tr><th>Claim Limitation (Claim 7)</th><th>Exemplary Disclosure</th></tr>
<tr><td></td><td>
The short-form floating-point format input signals represent a first numerical value having greater precision:

Example 1. $\overline{\text{STRB0}}$ and $\overline{\text{STRB1}}$ Data Access: Data Size = Memory Width

This example illustrates a savings in external memory by using bytes and half-words to store data that is less than 32 bits in size (see Figure 2). As in all cases, the data size and memory width for $\overline{\text{STRB0}}$ and $\overline{\text{STRB1}}$ data access cycles are configured in the corresponding strobe control registers (see Table 1).

The short program stored in the internal RAM0 memory begins with the LDI instruction reading an 8-bit integer from 8-bit-wide $\overline{\text{STRB0}}$ memory. As the integer data passes through the memory interface, it is sign-extended to 32 bits and loaded to R0 as a 32-bit integer. Next, the FLOAT instruction converts the integer in R0 to a 40-bit floating-point number and loads it to R1. Finally, the STF instruction truncates the 40-bit contents of R1 to 32 bits and stores it in the 16-bit-wide $\overline{\text{STRB1}}$ memory. As the data passes through the memory interface, the 24-bit mantissa is truncated to eight bits (the 8-bit exponent remains unmodified).

Table 1. $\overline{\text{STRB0}}$ and $\overline{\text{STRB1}}$ Data Access: Data Size = Memory Width

<table>
<tr><th></th><th>Strobe</th><th>Data Size</th><th>Memory Width</th></tr>
<tr><td>Input Data</td><td>$\overline{\text{STRB0}}$</td><td>8</td><td>8</td></tr>
<tr><td>Output Data</td><td>$\overline{\text{STRB1}}$</td><td>16</td><td>16</td></tr>
<tr><td>Program</td><td>RAM0</td><td>32</td><td>32</td></tr>
</table>

Interfacing Memory to the TMS320C32 DSP at 4.

This conversion to the 16-bit short-form floating-point format is also illustrated in Figure 2:
</td></tr>
</table>

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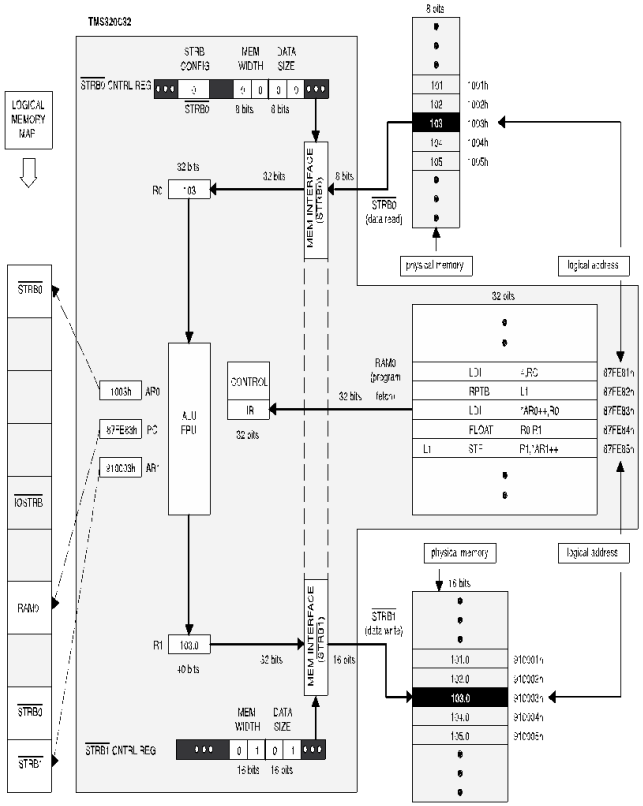
Claim Limitation (Claim 7)	Exemplary Disclosure
	 Figure 2. STRB0 and STRB1 Data Access: Data Size = Memory Width Interfacing Memory to the TMS320C32 DSP at 5.
[**156c**] wherein the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/1,000,000 through 1,000,000 and for at least X=5% of the possible valid inputs to the first operation, the	TI TMS320C32 discloses the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/1,000,000 through 1,000,000 and for at least X=5% of the possible valid inputs to the first operation, the statistical mean, over repeated execution of the first operation on each specific input from the at least X% of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least Y=0.05% from the result of an exact mathematical

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Claim Limitation (Claim 7)	Exemplary Disclosure
statistical mean, over repeated execution of the first operation on each specific input from the at least X% of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least Y=0.05% from the result of an exact mathematical calculation of the first operation on the numerical values of that same input;	calculation of the first operation on the numerical values of that same input. *See, e.g.*: *Floating-Point Formats* The following examples illustrate the range and precision of the 'C32 short floating-point format for external 16-bit data: Most positive: $x = (2-2^{-8}) \times 2^{127} = 3.3961775 \times 10^{38}$ Least positive $x = 1 \times 2^{-127} = 5.8774717541 \times 10^{-39}$ Least negative: $x = (-1-2^{-8}) \times 2^{-127} = -5.9004306 \times 10^{-39}$ Most negative: $x = (-2 \times 2^{127}) = -3.4028236 \times 10^{38}$ Note that the floating-point instructions (such as LDF, MPYF, ADDF) and the integer instructions (such as LDI, MPYI, ADDI) produce different results when accessing the same memory location. The *integer* load instructions store the value in the LSBs of the 'C32's registers. A bit field in the strobe control register controls sign extension or zero fill of the MSBs of the integer value. On the other hand, the *floating-point* load instructions store the value in the MSBs of the 'C32's registers. For example: If AR1 = 4000h, R1 = 00 00000000h, the value stored at memory location 4000h is 0180h, and $\overline{\text{STRB0}}$ is configured for a physical memory size and data type size of 16 bits. The result of: ADDI *AR1,R1 is R1 = 00 00000180h, while The result of: ADDF *AR1,R1 is R1 = 01 C0000000h (= – 3.0), since – 4.0 + 1.0 = – 3.0 TMS320C3x User's Guide 5-7; *see also supra* [156b]. For floating-point multiplication, the TI TMS320C32 operated as follows:

Exhibit 14 – TI TMS320C32

Claim Limitation (Claim 7)	Exemplary Disclosure
	During floating-point multiplication, source operands are in the single-precision floating-point format. If the source operands are in short floating-point format, they are converted to single-precision floating-point format. If the source operands are in extended-precision floating-point format, they are truncated to single-precision format. These conversions occur automatically in hardware with no overhead. All results of floating-point multiplications are in the extended-precision format. These multiplications occur in a single cycle. TMS320C3x User's Guide 5-26. That operation is also detailed in the flowchart and accompanying discussion:

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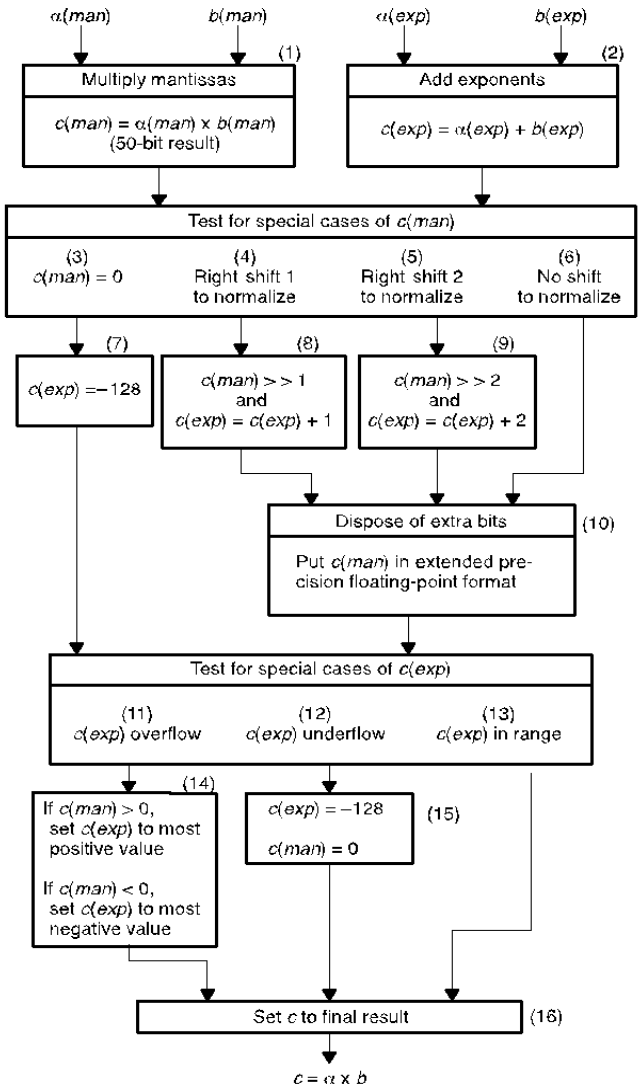
Claim Limitation (Claim 7)	Exemplary Disclosure
	Figure 5–16. Flowchart for Floating-Point Multiplication 

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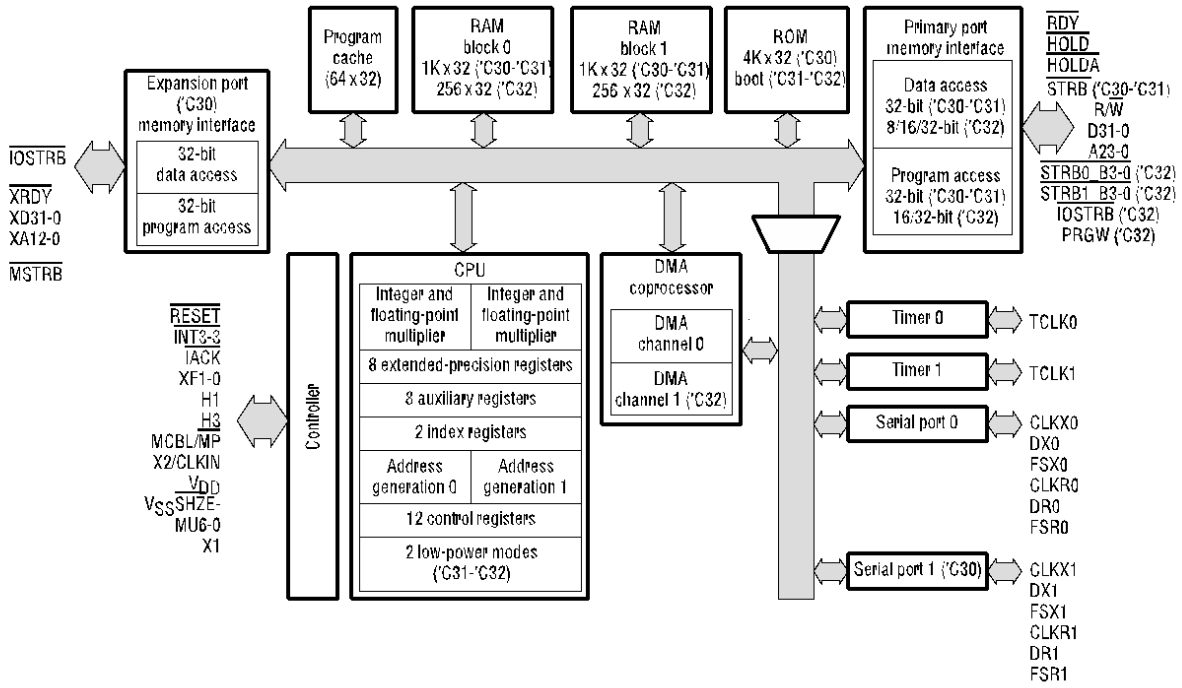
Claim Limitation (Claim 7)	Exemplary Disclosure
	TMS320C3x User's Guide 5-26 to 5-28. *See also* Appendix to Responsive Contentions Regarding Non-Infringement and Invalidity (detailing error rates associated with different mantissa sizes).
[**156d**] at least one first computing device adapted to control the operation of the at least one first LPHDR execution unit;	TI TMS320C32 discloses at least one first computing device adapted to control the operation of the at least one first LPHDR execution unit. *See, e.g.*: As reflected in the literature, the TI TMS320C32 had a CPU with the floating-point multiplier, which CPU had a controller; furthermore, the CPU itself controls the operation of its floating-point multipliers. *Figure 1–1. TMS320C3x Devices Block Diagram* 

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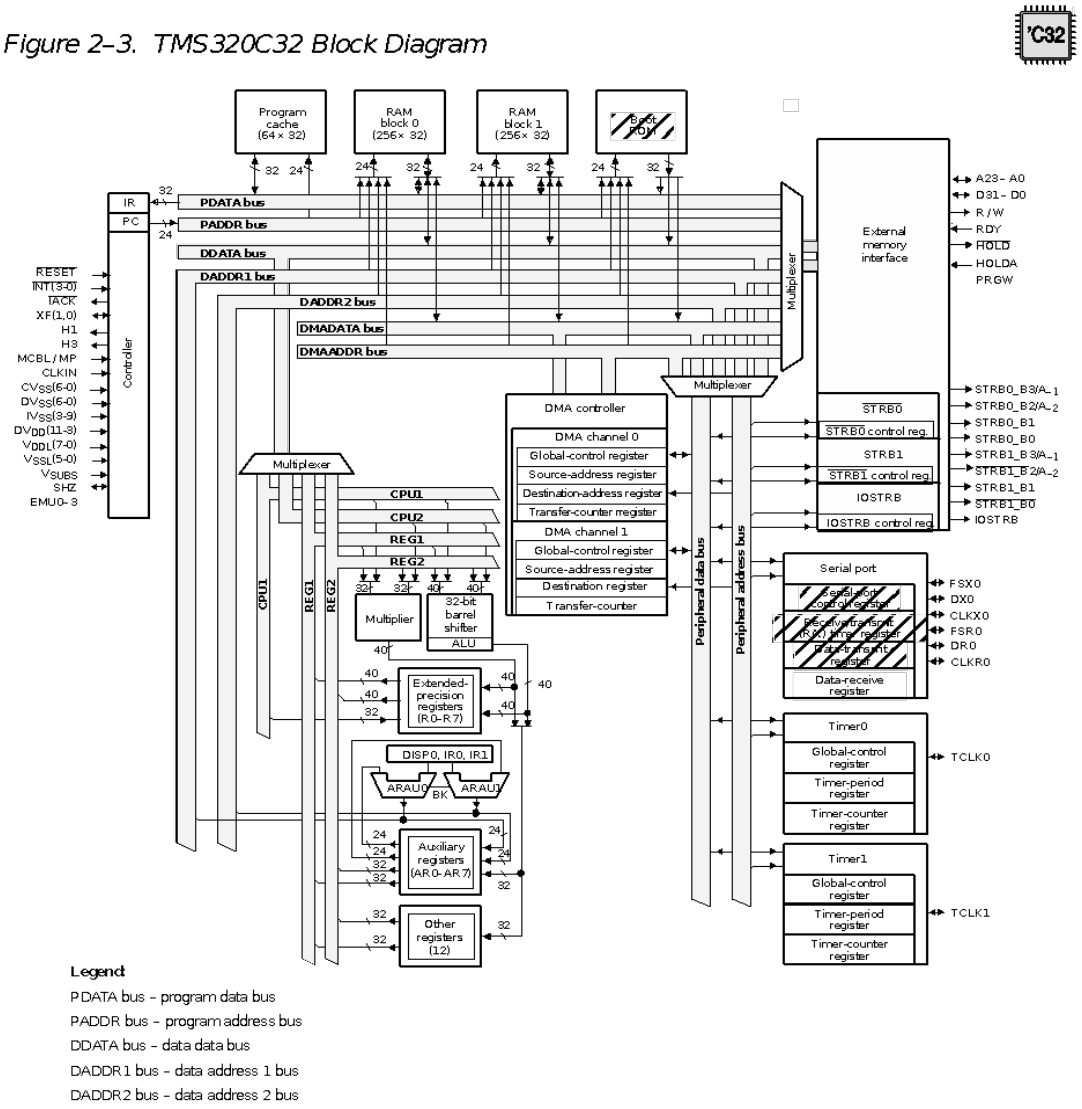
Claim Limitation (Claim 7)	Exemplary Disclosure
	TMS320C3x User's Guide 1-3.

Figure 2–3. TMS320C32 Block Diagram



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Claim Limitation (Claim 7)	Exemplary Disclosure
	TMS320C3x User's Guide 2-5.
[**156e**] wherein the at least one first computing device comprises at least one of a central processing unit (CPU), a graphics processing unit (GPU), a field programmable gate array (FPGA), a microcode-based processor, a hardware sequencer, and a state machine;	TI TMS320C32 discloses at least one first computing device comprises at least one of a central processing unit (CPU), a graphics processing unit (GPU), a field programmable gate array (FPGA), a microcode-based processor, a hardware sequencer, and a state machine. Specifically, the TMS320C32 discloses a CPU that controls the operation of its internal floating-point multipliers. At a minimum, one of skill in the art would have understood that the controllers of 156d were at least a state machine in the TMS320C32 chip.
[**156f**] and, wherein the number of LPHDR execution units in the device exceeds by at least one hundred the non-negative integer number of execution units in the device adapted to execute at least the operation of multiplication on floating point numbers that are at least 32 bits wide.	Based on the disclosure of the TI TMS320C32, it would have been obvious to one of skill in the art that the number of LPHDR execution units in the device could exceed by at least one hundred the non-negative integer number of execution units in the device adapted to execute at least the operation of multiplication on floating point numbers that are at least 32 bits wide. *See generally* Responsive Contentions Regarding Non-Infringement and Invalidity.

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'273 Patent

Claim Limitation (Claim 53)	Exemplary Disclosure
[**273a**] A device:	TI TMS320C32 discloses a device. *See* [**156a**].
[**273b**] comprising at least one first low precision high-dynamic range (LPHDR) execution unit adapted to execute a first operation on a first input signal representing a first numerical value to produce a first output signal representing a second numerical value,	TI TMS320C32 discloses at least one first low precision high-dynamic range (LPHDR) execution unit adapted to execute a first operation on a first input signal representing a first numerical value to produce a first output signal representing a second numerical value. *See* [**156b**].
[**273c**] wherein the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/1,000,000 through 1,000,000 and for at least X=5% of the possible valid inputs to the first operation, the statistical mean, over repeated execution of the first operation on each specific input from the at least X % of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least Y=0.05% from the result of an exact mathematical calculation of the first operation on the numerical values of that same input;	TI TMS320C32 discloses the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/1,000,000 through 1,000,000 and for at least X=5% of the possible valid inputs to the first operation, the statistical mean, over repeated execution of the first operation on each specific input from the at least X % of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least Y=0.05% from the result of an exact mathematical calculation of the first operation on the numerical values of that same input. *See* [**156c**].
[**273d**] wherein the number of LPHDR execution units in the device exceeds by at least one hundred the non-negative integer number of execution units in the device adapted to execute at least the operation of multiplication on floating point numbers that are at least 32 bits wide.	Based on the disclosure of the TI TMS320C32, it would have been obvious to one of skill in the art that the number of LPHDR execution units in the device could exceed by at least one hundred the non-negative integer number of execution units in the device adapted to execute at least the operation of multiplication on floating point numbers that are at least 32 bits wide. *See* [**156f**].

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'961 Patent

Claim Limitation (Claim 4)	Exemplary Disclosure
[**961a**] A device comprising:	TI TMS320C32 discloses a device. *See* [**156a**].
[**961b**] at least one first low precision high-dynamic range (LPHDR) execution unit adapted to execute a first operation on a first input signal representing a first numerical value to produce a first output signal representing a second numerical value,	TI TMS320C32 discloses at least one first low precision high-dynamic range (LPHDR) execution unit adapted to execute a first operation on a first input signal representing a first numerical value to produce a first output signal representing a second numerical value. *See* [**156b**].
[**961c**] wherein the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/1,000,000 through 1,000,000 and for at least X=10% of the possible valid inputs to the first operation, the statistical mean, over repeated execution of the first operation on each specific input from the at least X% of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least Y=0.2% from the result of an exact mathematical calculation of the first operation on the numerical values of that same input; and	TI TMS320C32 discloses the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/1,000,000 through 1,000,000 and for at least X=10% of the possible valid inputs to the first operation, the statistical mean, over repeated execution of the first operation on each specific input from the at least X% of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least Y=0.2% from the result of an exact mathematical calculation of the first operation on the numerical values of that same input. *See* [**156c**].
[**961d**] at least one first computing device adapted to control the operation of the at least one first LPHDR execution unit.	TI TMS320C32 discloses at least one first computing device adapted to control the operation of the at least one first LPHDR execution unit. *See* [**156d**].

Exhibit 14 – TI TMS320C32

Claim Limitation (Claim 13)	Exemplary Disclosure
[**961e**] A device comprising:	TI TMS320C32 discloses a device. *See* [**156a**].
[**961f**] a plurality of components comprising:	TI TMS320C32 discloses a plurality of components. *See* [**156b**] + **[156d]**.
[**961g**] at least one first low precision high-dynamic range (LPHDR) execution unit adapted to execute a first operation on a first input signal representing a first numerical value to produce a first output signal representing a second numerical value,	TI TMS320C32 discloses at least one first low precision high-dynamic range (LPHDR) execution unit adapted to execute a first operation on a first input signal representing a first numerical value to produce a first output signal representing a second numerical value. *See* [**156b**]
[**961h**] wherein the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/1,000,000 through 1,000,000 and for at least X=10% of the possible valid inputs to the first operation, the statistical mean, over repeated execution of the first operation on each specific input from the at least X% of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least Y=0.2% from the result of an exact mathematical calculation of the first operation on the numerical values of that same input.	TI TMS320C32 discloses the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/1,000,000 through 1,000,000 and for at least X=10% of the possible valid inputs to the first operation, the statistical mean, over repeated execution of the first operation on each specific input from the at least X% of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least Y=0.2% from the result of an exact mathematical calculation of the first operation on the numerical values of that same input. *See* [**156c**].